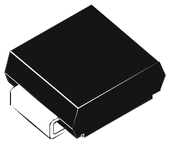
SMP100LC

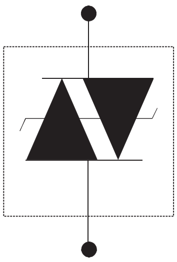
Trisil™ for telecom equipment protection

Features

- Bidirectional crowbar protection
- Voltage range from 8 V to 400 V
- Low capacitance from 20 pF to 45 pF @ 50 V
- Low leakage current : I_R = 2 µA max
- Holding current: I_H = 150 mA min
- Repetitive peak pulse current:
  I_{PP} = 100 A (10/1000 µs)



SMB
(JEDEC DO-214AA)



Main applications

Any sensitive equipment requiring protection against lightning strikes and AC power faults.

These devices are dedicated to central office protection as they comply with the most stressfull standards.

Their Low Capacitances make them suitable for xDSL.

Description

The SMP100LC is a series of low capacitance transient surge arrestors designed for the protection of high data rate communication equipment. Its low capacitance avoids any distortion of the signal and is compatible with digital transmission line cards (xDSL, ISDN...).

SMP100LC series tested and confirmed compatible with Cooper Bussmann Telecom Circuit Protector TCP 1.25A.

The SMP100LC-xxx with the fuse TCP1.25A or TCP2A is compliant with Telcordia GR1089 (lightning and AC power fault tests), ITU-T K20/K21 (lightning and AC power fault tests), TIA/EIA-IS-968 (formely FCC Part 68 lightning tests), UL60950 (AC power fault tests).

Moreover, the use of the TCP1.25A allows the SMP100LC-xxx to be safe for the 2nd level (B criteria) AC power fault tests.

Order Code

Order code	Marking
SMP100LC-xxx	See *Section 5 on page 11*

Benefits

Trisils are not subject to ageing and provide a fail safe mode in short circuit for a better protection. They are used to help equipment to meet main standards such as UL60950, IEC950 / CSA C22.2 and UL1459. They have UL94 V0 approved resin. SMB package is JEDEC registered (DO-214AA). Trisils comply with the following standards GR-1089 Core, ITU-T-K20/K21, VDE0433, VDE0878, IEC61000-4-5 and FCC part 68.

1 Characteristics

Table 1. Compliant with the following standards

STANDARD	Peak Surge Voltage (V)	Waveform Voltage	Required peak current (A)	Current waveform	Minimum serial resistor to meet standard (Ω)
GR-1089 Core First level	2500 1000	2/10 µs 10/1000 µs	500 100	2/10 µs 10/1000 µs	0 0
GR-1089 Core Second level	5000	2/10 µs	500	2/10 µs	0
GR-1089 Core Intra-building	1500	2/10 µs	100	2/10 µs	0
ITU-T-K20/K21	6000 1500	10/700 µs	150 37.5	5/310 µs	0 0
ITU-T-K20 (IEC61000-4-2)	8000 15000	1/60 ns	ESD contact discharge ESD air discharge		0 0
VDE0433	4000 2000	10/700 µs	100 50	5/310 µs	0 0
VDE0878	4000 2000	1.2/50 µs	100 50	1/20 µs	0 0
IEC61000-4-5	4000 4000	10/700 µs 1.2/50 µs	100 100	5/310 µs 8/20 µs	0 0
FCC Part 68, lightning surge type A	1500 800	10/160 µs 10/560 µs	200 100	10/160 µs 10/560 µs	0 0
FCC Part 68, lightning surge type B	1000	9/720 µs	25	5/320 µs	0

Table 2. Absolute ratings (T_{amb} = 25° C)

Symbol	Parameter		Value	Unit
I_{PP}	Repetitive peak pulse current (see *Figure 1*)	10/1000 µs 8/20 µs 10/560 µs 5/310 µs 10/160 µs 1/20 µs 2/10 µs	100 400 140 150 200 400 500	A
I_{FS}	Fail-safe mode : maximum current [(1)]	8/20 µs	5	kA
I_{TSM}	Non repetitive surge peak on-state current (sinusoidal)	t = 0.2 s t = 1 s t = 2 s t = 15 mn	24 15 12 4	A
I^2t	I^2t value for fusing	t = 16.6 ms t = 20 ms	20 21	A^2s
T_{stg} T_j	Storage temperature range Maximum junction temperature		-55 to 150 150	° C
T_L	Maximum lead temperature for soldering during 10 s.		260	° C

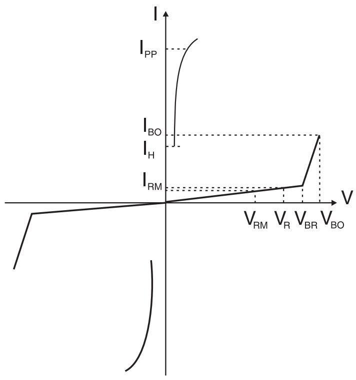
1. in fail safe mode, the device acts as a short circuit

Table 3. Thermal Resistances

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction to ambient (with recommended footprint)	100	° C/W
$R_{th(j-l)}$	Junction to leads	20	° C/W

Table 4. Electrical Characteristics (T_{amb} = 25° C)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_{RM}	Leakage current
I_{PP}	Peak pulse current
I_{BO}	Breakover current
I_H	Holding current
V_R	Continuous reverse voltage
I_R	Leakage current at V_R
C	Capacitance



Type	I_{RM} @ V_{RM} max. µA	V_{RM} V	I_R @ V_R (1) max. µA	V_R V	Dynamic V_{BO} (2) max. V	Static V_{BO} @ I_{BO} (3) max. V	I_{BO} max. mA	I_H (4) min. mA	C(5) typ. pF	C(6) typ. pF
SMP100LC-8		6		8	25	15		50 (typ.)	NA	75
SMP100LC-25		22		25	40	35			NA	65
SMP100LC-35		32		35	55	55			NA	55
SMP100LC-65		55		65	85	85			45	90
SMP100LC-90		81		90	120	125			40	80
SMP100LC-120		108		120	155	150			35	75
SMP100LC-140	2	126	5	140	180	175	800	150	30	65
SMP100LC-160		144		160	205	200			30	65
SMP100LC-200		180		200	255	250			30	60
SMP100LC-230		207		230	295	285			30	60
SMP100LC-270		243		270	345	335			30	60
SMP100LC-320		290		320	400	390			25	50
SMP100LC-360		325		360	460	450			25	50
SMP100LC-400		360		400	540	530			20	45

1. I_R measured at V_R guarantee V_{BR} min ≥ V_R
2. See *Figure 15: Test circuit 1 for Dynamic I_{BO} and V_{BO} parameters*
3. See *Figure 16: Test circuit 2 for I_{BO} and V_{BO} parameters*
4. See *Figure 17: Test circuit 3 for dynamic I_H parameter*
5. V_R = 50 V bias, V_{RMS} =1 V, F = 1 MHz
6. V_R = 2V bias, V_{RMS} =1 V, F = 1 MHz

Figure 1. Pulse waveform

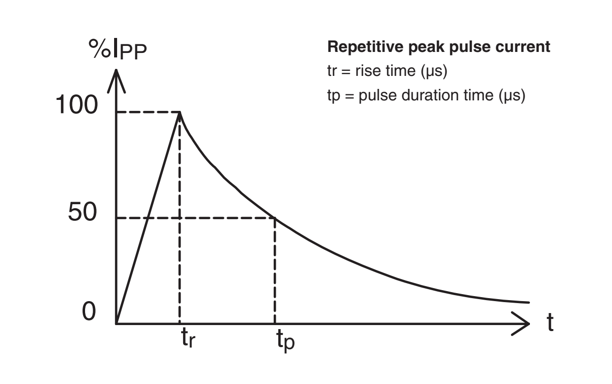


Figure 2. Non repetitive surge peak on-state current versus overload duration

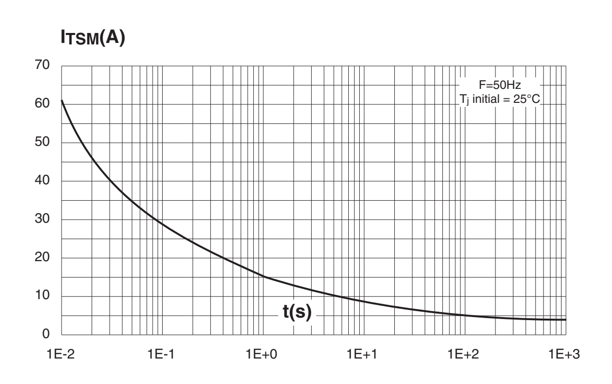


Figure 3. On-state voltage versus on-state current (typical values)

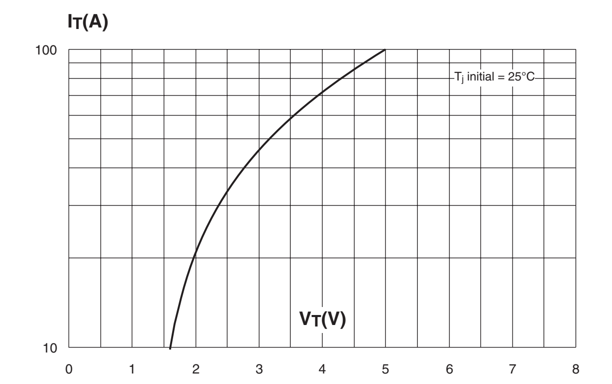


Figure 4. Relative variation of holding current versus junction temperature

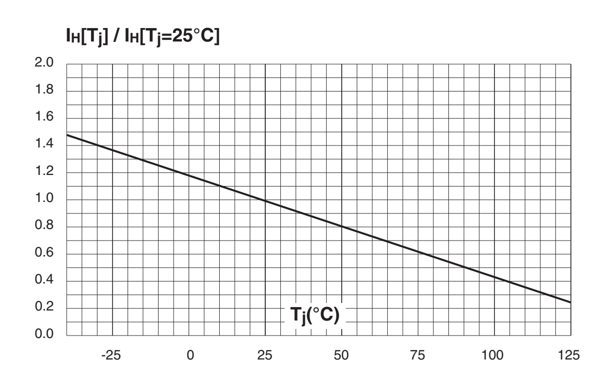


Figure 5. Relative variation of breakover voltage versus junction temperature

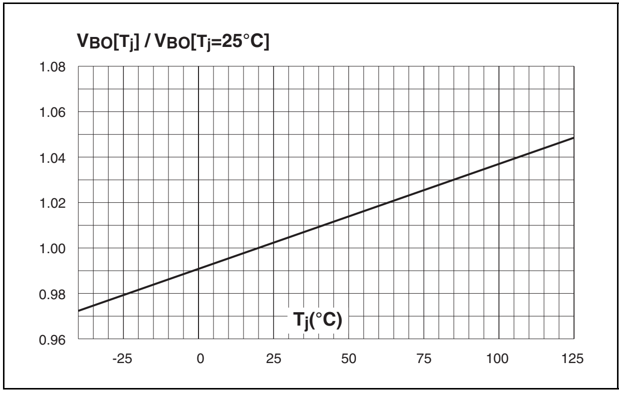


Figure 6. Relative variation of leakage current versus junction temperature (typical values)

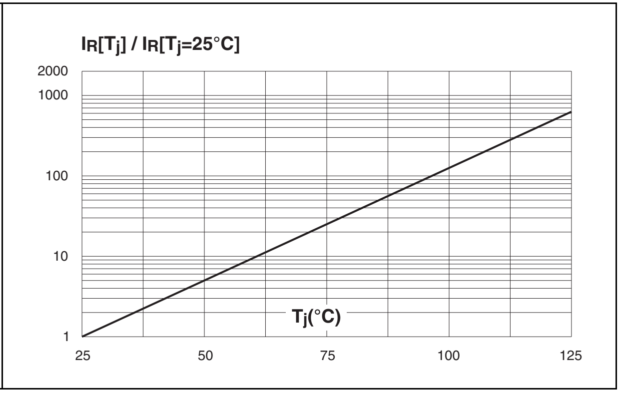


Figure 7. Variation of thermal impedance junction to ambient versus pulse duration (PCB - FR4, S_{Cu} = 35µm, recommended pad layout)

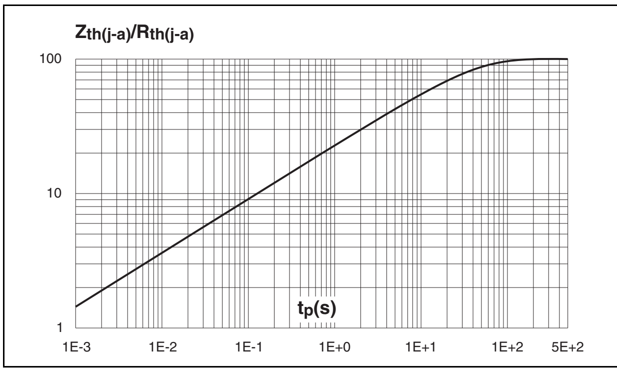
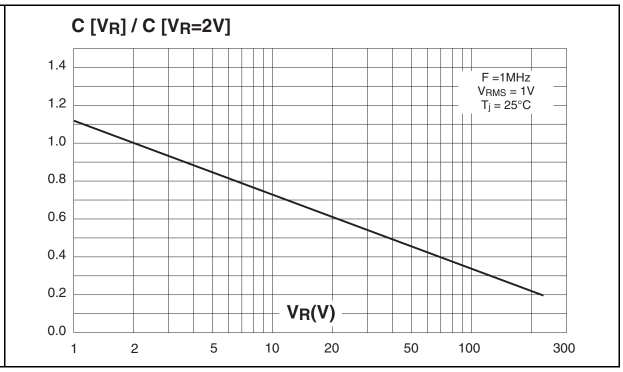


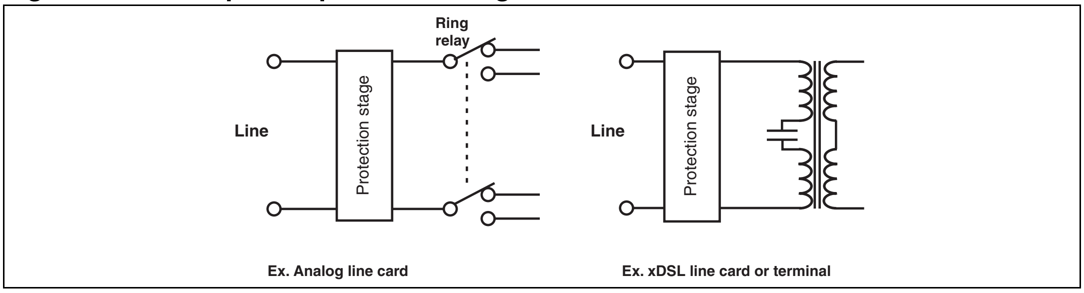
Figure 8. Relative variation of junction capacitance versus reverse voltage applied (typical values)



2 Application information

In wireline applications, analog or digital, both central office and subscriber sides have to be protected. This function is assumed by a combined series / parallel protection stage.

Figure 9. Examples of protection stages for line cards



In such a stage, parallel function is assumed by one or several Trisil, and is used to protect against short duration surge (lightning). During this kind of surges the Trisil limits the voltage across the device to be protected at its break over value and then fires. The fuse assumes the series function, and is used to protect the module against long duration or very high current mains disturbances (50/60Hz). It acts by safe circuit opening. Lightning surge and mains disturbance surges are defined by standards like GR1089, FCC part 68, ITU-T K20.

Figure 10. Typical circuits

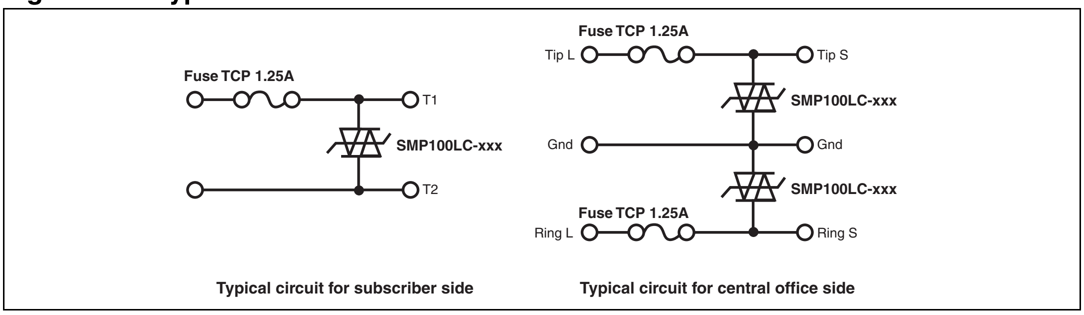
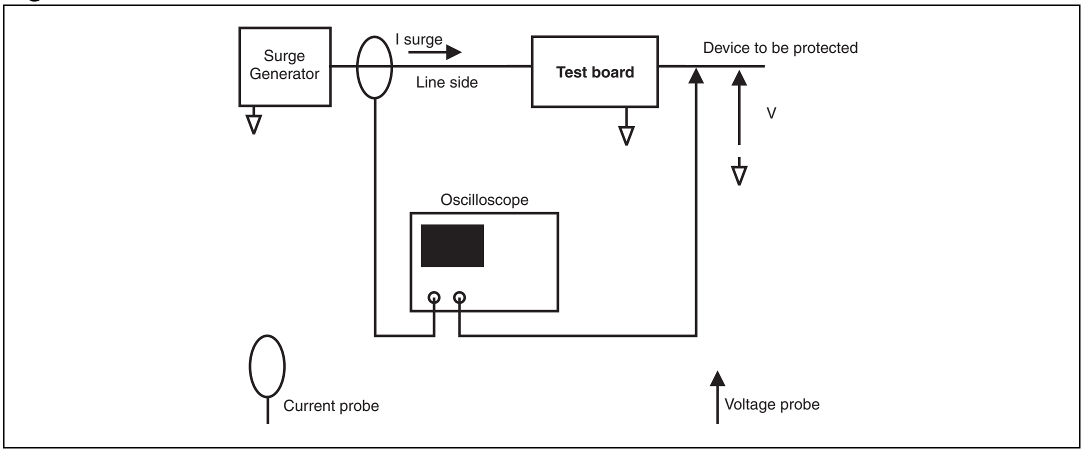
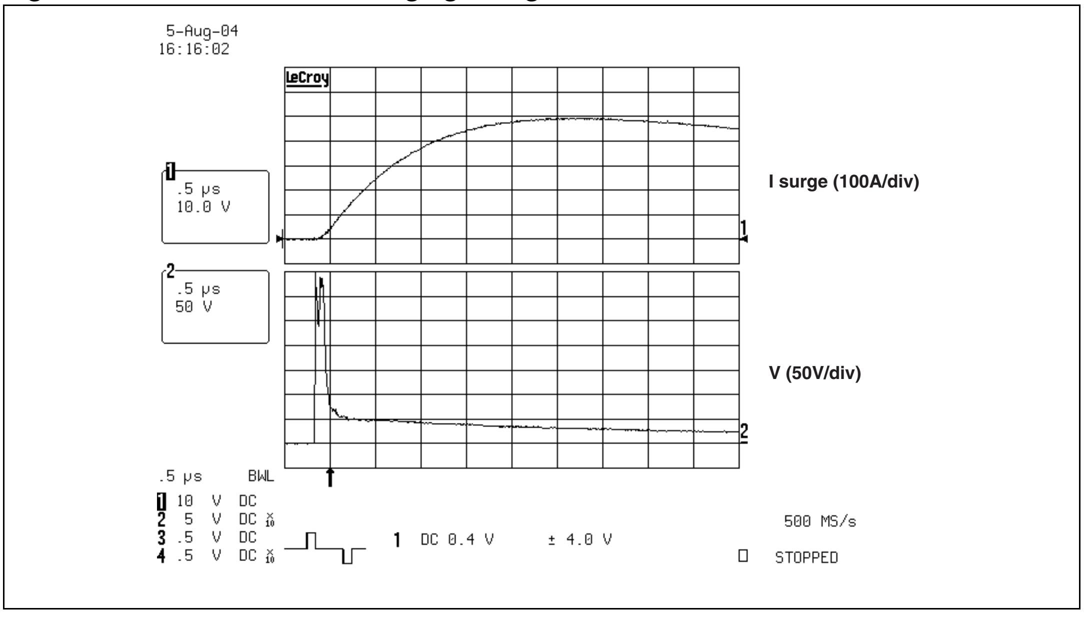


Figure 11. Test method of the board with fuse and Trisil



These topologies, using SMP100LC from ST and TCP1.25A from Cooper Bussmann, have been functionally validated with a Trisil glued on the PCB. Following example was performed with SMP100LC-270 Trisil. For more information, see Application Note AN2064.

Figure 12. Trisil turns on during lightning strike



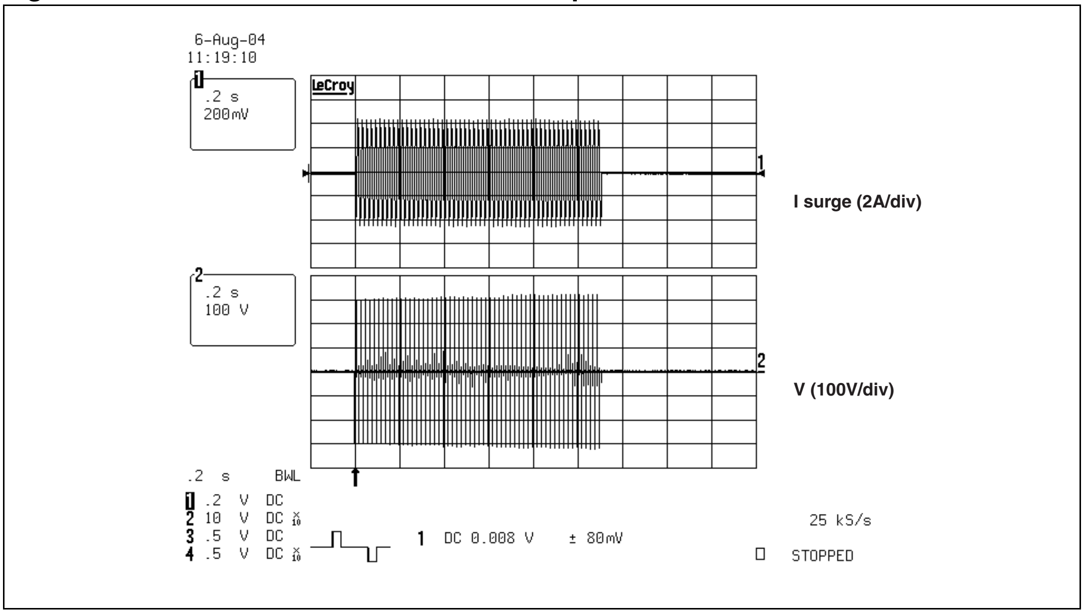
Test conditions:

2/10 µs + and - 2.5 and 5 kV, 500 A (10 pulses of each polarity), T_{amb} = 25° C

Test result:

Fuse and Trisil OK after test in accordance with GR1089 requirements.

Figure 13. Trisil action while fuse remains operational



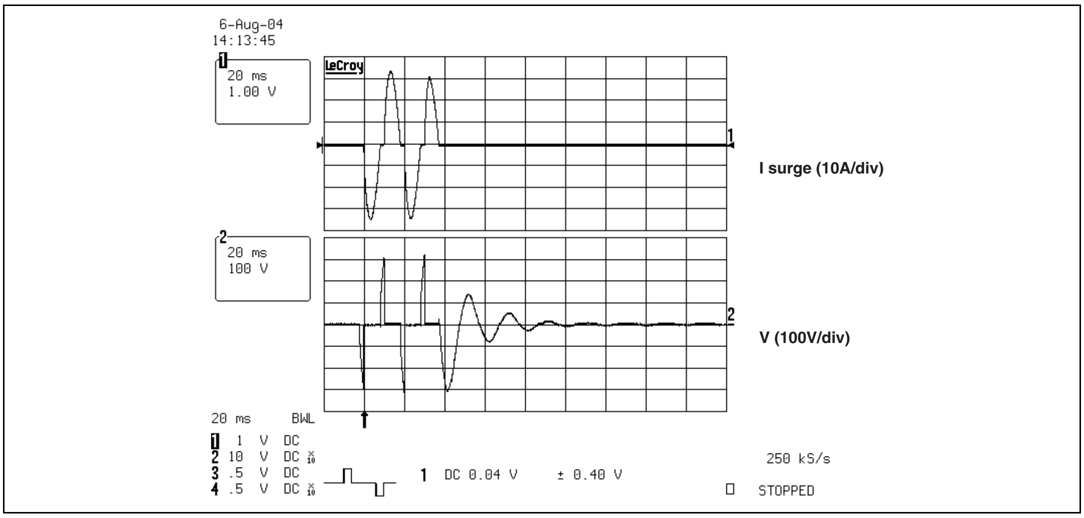
Test conditions:

600 V, 3 A, 1.1 s (first level), T_{amb} = 25° C

Test result:

Fuse and Trisil OK after test in accordance with GR1089 requirements.

Figure 14. High current AC power test: the fuse acts like a switch by opening the circuit



Test conditions:

277 V, 25 A (second level), T_{amb} = 25° C

Test result:

Fuse safely opened and Trisil OK after test in accordance with GR1089 requirements.

Figure 15. Test circuit 1 for Dynamic I_{BO} and V_{BO} parameters

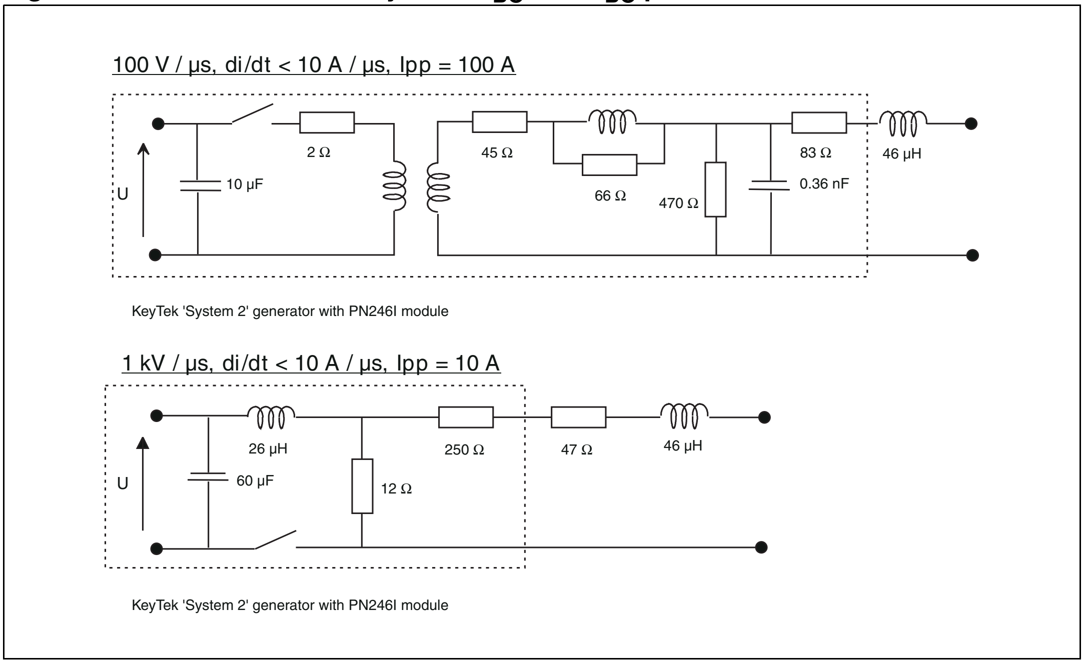
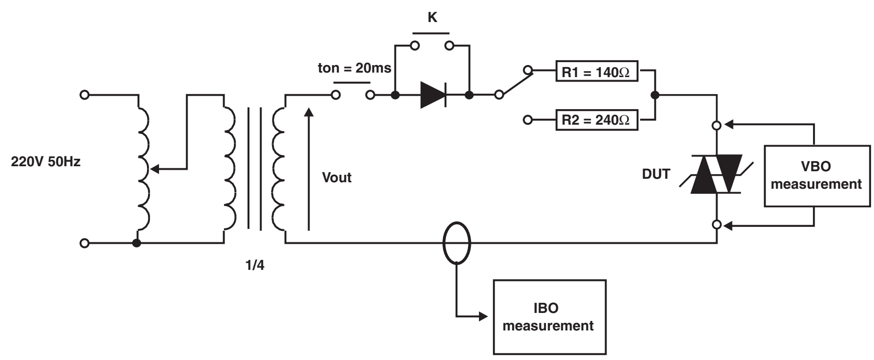


Figure 16. Test circuit 2 for I_{BO} and V_{BO} parameters



TEST PROCEDURE

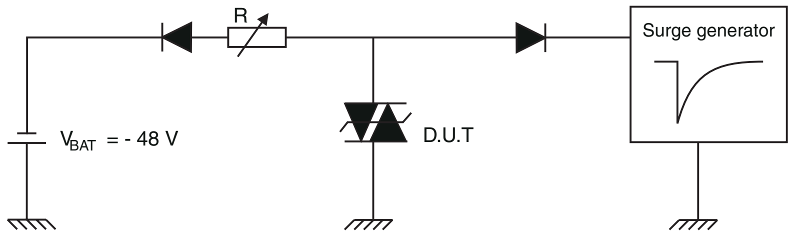
Pulse test duration (tp = 20ms):

- for Bidirectional devices = Switch K is closed
- for Unidirectional devices = Switch K is open

V_{OUT} selection:

- Device with V_{BO} < 200V → V_{OUT} = 250 V_{RMS}, R1 = 140Ω
- Device with V_{BO} ≥ 200V → V_{OUT} = 480 V_{RMS}, R2 = 240Ω

Figure 17. Test circuit 3 for dynamic I_H parameter



This is a GO-NOGO test which allows to confirm the holding current (I_H) level in a functional test circuit.

TEST PROCEDURE

1/ Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2/ Fire the D.U.T. with a surge current → I_{PP} = 10A, 10/1000µs.
3/ The D.U.T. will come back off-state within 50ms maximum.

3 Ordering information scheme

SMP 100 LC - xxx

Trisil Surface Mount

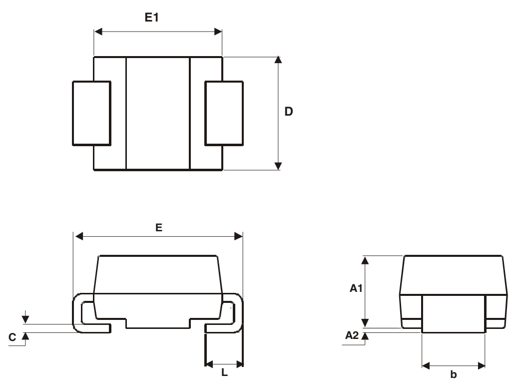
Repetitive Peak Pulse Current
100 = 100A

Capacitance
LC = Low Capacitance

Voltage
65 = 65V

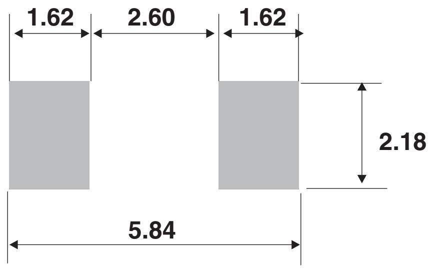
4 Package information

Table 5. SMB Dimensions



Ref.	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A1	1.90	2.45	0.075	0.096
A2	0.05	0.20	0.002	0.008
b	1.95	2.20	0.077	0.087
c	0.15	0.40	0.006	0.016
E	5.10	5.60	0.201	0.220
E1	4.05	4.60	0.159	0.181
D	3.30	3.95	0.130	0.156
L	0.75	1.50	0.030	0.059

Figure 18. Footprint (dimensions in mm)



5 Ordering information

Part Number	Marking	Package	Weight	Base qty	Delivery mode
SMP100LC-8	PL8	SMB	0.11 g	2500	Tape & reel
SMP100LC-25	L25				
SMP100LC-35	L35				
SMP100LC-65	L06				
SMP100LC-90	L09				
SMP100LC-120	L12				
SMP100LC-140	L14				
SMP100LC-160	L16				
SMP100LC-200	L20				
SMP100LC-230	L23				
SMP100LC-270	L27				
SMP100LC-320	L32				
SMP100LC-360	L36				
SMP100LC-400	L40				

6 Revision history

Date	Revision	Changes
09-Nov-2004	9	Absolute ratings values, table 3 on page 2, updated.
07-Dec-2004	10	SMP100LC-320, SMP100LC-360 and SMP100LC-400 addition.
20-Jun-2005	11	Telecom Circuit Protector added in *Description*.
05-Mar-2007	12	Reformatted to current standards. SMB *Package information* updated. Standards compliance paragraphs added to *Description*

Please Read Carefully: